AMENDMENTS

In the Claims:

This listing of claims replaces all prior versions and listings of the claims in the application.

1. (currently amended)   An apparatus ~~for~~ performing the addition of a propagate, kill, and generate ~~PKG~~ recoded number~~s~~, said apparatus comprising:

a circuitry configured to receive at least a first ~~value~~ operand and a second ~~value~~ operand, the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations of respective first and second binary operands; ~~and~~

a first carry-save adder configured to add said first ~~value~~ operand and said second ~~value~~ operand, ~~wherein said second value is at least one of a P value, a K value, and a G value of a~~ PKG ~~recoded number and said first adder~~ to generate~~s~~ a ~~carry-out value and at least one of a P value, a K value and G value of a~~ third ~~PKG~~ propagate, kill, and generate recoded number representation; and ~~wherein said circuitry generates a sum value and a carry value~~

a modified carry-save adder configured to receive the third propagate, kill, and generate recoded number representation, add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation, and generate a sum value and a carry value.

2. (original)   The apparatus of claim 1, wherein said sum value and said carry value are dual rail encoded values.

3. (previously canceled)

4. (currently amended)   The apparatus of claim 1, wherein said circuitry ~~further comprises:~~ is configured to receive and apply a carry-in value to the modified carry-save adder ~~a second adder configured to add said PKG recoded number from said first adder and a carry-in value.~~

5. - 6. (canceled)

7.   (presently amended)   A method for ~~performing the addition of PKG~~ processing propagate, kill, and generate representations of respective first and second binary operands ~~recoded numbers~~, comprising:

receiving ~~a first value~~ a carry-in value and a first and a second propagate, kill, and generate representation of respective first and second binary operands;

adding the first and second propagate, kill, and generate representations to generate a third propagate, kill, and generate representation; and

mathematically combining the third propagate, kill, and generate representation and the carry-in value to generate a sum value and a carry value ~~receiving a second value, wherein said second value is at least one of a P value, a K value, and a G value of a first PKG recoded number; and~~

~~generating a sum value including at least one of a P value, a K value and G value of a second PKG recoded number and a first carry-out value from said first value and said second value~~.

8.   (presently amended)   The method of claim 7, wherein said step of mathematically combining comprises adding the third propagate, kill, and generate representation and the carry-in value ~~further comprising:~~

~~forwarding a first result including at least one of a P value, a K value and a G value from said generating~~.

9.   (canceled)

10.   (presently amended)   The method of claim ~~9~~ 7, wherein said step of mathematically combining further comprises generating ~~final sum value and said final carry-out value~~ dual rail encoded values.

11.   (presently amended)   The method of ~~claim 8~~ claim 7, further comprising: generating a carry-out value responsive to the adding ~~wherein said first value is a PKG value~~.

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12. - 13.   (canceled)

14.   (previously canceled)

15. - 19.   (canceled)

20. - 21   (previously canceled)

22.   (canceled)